In the Claims:

1. (Original) A multiprocessor control block for use in a communication switch, comprising:

a resource routing processor that controls resource allocation amongst connections supported by the switch and routing functionality corresponding to at least a portion of the connections supported by the switch;

a plurality of intermediate processors operably coupled to the resource routing processor, wherein each intermediate processor of the plurality of intermediate processors performs call processing for a corresponding portion of the connections supported by the switch, wherein call processing includes issuing resource allocation requests to the resource routing processor, wherein each intermediate processor of the plurality of intermediate processors performs functions associated with a signaling layer portion of a protocol stack; and

a link layer processor operably coupled to the plurality of intermediate processors, wherein the link layer processor is operable to couple to a switching fabric of the communication switch, wherein the link layer processor receives ingress data units from the switching fabric and selectively forwards each ingress data unit received to at least one of the plurality of intermediate processors, wherein the link layer processor receives egress data units from the plurality of intermediate processors and forwards each of the egress data units to the switching fabric.

2. (Original) The multiprocessor control block of claim 1, wherein resource allocation includes allocation of channels within the switch.

3. (Original) The multiprocessor control block of claim 1, wherein resource allocation includes allocation of bandwidth within the switch.

4. (Original) The multiprocessor control block of claim 1, wherein call processing includes handling subscriber features.

5. (Original) The multiprocessor control block of claim 1, wherein the ingress and egress data units include asynchronous transfer mode (ATM) cells.

6. (Original) The multiprocessor control block of claim 5, wherein the ingress and egress data units include ATM adaption layer 5 (AAL5) packets.

7. (Original) The multiprocessor control block of claim 1, wherein the ingress and egress data units include Internet Protocol (IP) packets.

8. (Original) The multiprocessor control block of claim 1, wherein the link layer processor performs link management functions.

9. (Original) The multiprocessor control block of claim 1, wherein the link layer processor selectively forwards at least a portion of the ingress data units based on a prioritization scheme.

10. (Original) The multiprocessor control block of claim 9, wherein the prioritization scheme is a round-robin scheme.

11. (Original) The multiprocessor control block of claim 9, wherein the prioritization scheme is at least partially based on loading on each intermediate processor of the plurality of intermediate processors.

12. (Original) The multiprocessor control block of claim 1, wherein each ingress data unit corresponding to a particular call is assigned a sequence number corresponding to the particular call.

13. (Original) The multiprocessor control block of claim 1, wherein the link layer processor forwards ingress data units corresponding to a global call message to each intermediate processor of the plurality of intermediate processors.

14. (Original) The multiprocessor control block of claim 1, wherein the link layer processor collects responses to the global call message from each intermediate processor of the plurality of intermediate processors and compiles the responses to produce a unified response.

15. (Original) The multiprocessor control block of claim 1 further comprises a message processor operably coupled to the plurality of intermediate processors, wherein the message processor supports messaging between the plurality of intermediate processors and at least one line card.

16. (Original) The multiprocessor control block of claim 15, wherein the message processor acts as a queuing point for messages between the plurality of intermediate processors and the at least one line card.

17. (Original) The multiprocessor control block of claim 1 further comprises a management block operably coupled to the resource routing processor, the plurality of intermediate processors, and the link layer processor, wherein the management block receives management requests and issues configuration commands to the resource routing processor, the plurality of intermediate processors, and the link layer processor based on the management requests.

18. (Original) The multiprocessor control block of claim 1 further comprises:

a second plurality of intermediate processors operably coupled to the resource routing processor, wherein each intermediate processor of the second plurality of intermediate processors performs call processing for a second corresponding portion of the connections supported by the switch, wherein call processing includes issuing resource allocation requests to the resource routing processor, wherein each intermediate processor of the plurality of intermediate processors performs functions associated with a signaling layer portion of the protocol stack; and

a second link layer processor operably coupled to the second plurality of intermediate processors, wherein the second link layer processor is operable to couple to the switching fabric of the communication switch, wherein the second link layer processor receives ingress data units from the switching fabric and selectively forwards each ingress data unit received to at least one intermediate

processor of the second plurality of intermediate processors, wherein the second link layer processor receives egress data units from the second plurality of intermediate processors and forwards each of the egress data units to the switching fabric.

19. (Original) A communication switch, comprising:

a switching fabric;

a plurality of line cards operably coupled to the switching fabric; and

a multiprocessor control block operably coupled to the switching fabric and the plurality of line cards, wherein the multiprocessor control block includes:

a resource routing processor that controls resource allocation amongst connections supported by the switch and routing functionality corresponding to at least a portion of the connections supported by the switch;

a plurality of intermediate processors operably coupled to the resource routing processor, wherein each intermediate processor of the plurality of intermediate processors performs call processing for a corresponding portion of the connections supported by the switch, wherein call processing includes issuing resource allocation requests to the resource routing processor, wherein each intermediate processor of the plurality of intermediate processors performs functions associated with a signaling layer portion of a protocol stack; and

a link layer processor operably coupled to the plurality of intermediate processors, wherein the link layer processor is operable to couple to the switching fabric of the communication switch, wherein the link layer processor receives ingress data units from the switching fabric and selectively forwards each ingress data unit received to at least one of the plurality of intermediate processors, wherein the link layer processor receives egress data units from the plurality of intermediate processors and forwards each of the egress data units to the switching fabric.

20. (Original) The communication switch of claim 19, wherein the multiprocessor control block further comprises a message processor operably coupled the multiprocessor management block and the plurality of line cards, wherein the message processor supports messaging between the plurality of intermediate processors and the plurality of line cards.

21. (Original) The communication switch of claim 19, wherein the multiprocessor control block further comprises a management block operably coupled to the resource routing processor, the plurality of intermediate processors, and the link layer processor, wherein the management block receives management requests and issues configuration commands to the resource routing processor, the plurality of intermediate processors, and the link layer processor based on the management requests.

22. (Original) The communication switch of claim 21, wherein the management block is operably coupled to the plurality of line cards, wherein the management block issues configuration commands to at least one of the plurality of line cards.

23. (Original) The communication switch of claim 19, wherein the ingress and egress data units include asynchronous transfer mode (ATM) cells.

24. (Currently amended) A method for processing ingress data units in a link layer processor of a multiprocessor control block in a communication switch, comprising:

receiving a first ingress data unit corresponding to a call;

selecting a first selected intermediate processor of a plurality of intermediate processors included in the multiprocessor control block, wherein selecting a first selected intermediate processor includes selecting a plurality of selected intermediate processors from the plurality of intermediate processors based on a global call reference included in the first ingress data unit; and

forwarding the first ingress data unit to the first selected intermediate processor, wherein forwarding the first ingress data unit includes forwarding the first ingress data unit to the plurality of selected intermediate processors.

25. (Original) The method of claim 24, wherein selecting the first selected intermediate processor further comprises selecting the first selected intermediate processor based on a prioritization scheme.

26. (Original) The method of claim 25, wherein the prioritization scheme includes a round robin scheme.

27. (Original) The method of claim 25, wherein the prioritization scheme is at least partially based on loading on each intermediate processor of the plurality of intermediate processors.

28. (Original) The method of claim 24 further comprises assigning a sequence number to the first ingress data unit, wherein the sequence number corresponds to the call.

29. (Original) The method of claim 28 further comprises:

receiving a second ingress data unit corresponding to the call;

assigning the sequence number corresponding to the call to the second ingress data unit;

selecting a second selected intermediate processor of the plurality of intermediate processors; and

forwarding the second ingress data unit to the second selected intermediate processor.

30. (Canceled)

31. (Currently amended) The method of claim ~~30~~ 24 further comprises:

collecting responses to the global call reference from each intermediate processor of the plurality of selected intermediate processors; and

compiling the responses to produce a unified response.